ABSTRACT

A process for fabricating input/output, N channel, (I/O NMOS) devices, featuring an ion implanted nitrogen region, used to reduce hot carrier electron, (HCE), injection, has been developed. The process features implanting a nitrogen region, at the interface of an overlying silicon oxide layer, and an underlying lightly doped source/drain, (LDD); region. The implantation procedure can either be performed prior to, or after, the deposition of a silicon oxide liner layer, in both cases resulting in a desired nitrogen pile-up at the oxide - LDD interface, as well as resulting in a more graded LDD profile. An increase in the time to fail, in regards to HCE injection, for these I/O NMOS devices, is realized, when compared to counterparts fabricated without the nitrogen implantation procedure.